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KONTRON ELECTRONIC GROUP

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KLA

8085 DISASSEMBLER

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(PRELIMINARY)

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KONTRON MESSTECHNIK GmbH, Breslauer Str.2, 8057 Eching/Munich, BRD.

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1. Introduction

The 8085 disassembler is an option to the KLA series logic analyzers which allows to analyse circuits based on the Intel 8085 microprocessor family in a simple and convenient way. The powerful features of the basic KLA logic analyzer are kept fully.

The disassembler occupies at least 24 channels (3 normal data probes) and one clock probe. Using a fourth data probe, further lines of the microprocessor can be controlled.

For the use of the disassembler, the explanations given in the KLA operating manual fully apply.

2. Components of the 8085 Disassembler

Further to the KLA itself, including 4 probes (3 data, 1 clock), the listed components are needed:

(1) 8085 personality probe consisting of:
   a) 1 UPR-6 or UPR-10 Universal Probe Rack
   b) 1 C-8085 Configurator
   c) 1 Clip-40, ribbon cable with 40 IC- clip
   d) 1 Multiclock probe configured for 8085

(2) 1 8085 disassembler software on KLA- diskette

3. Theory of Operation

3.1 Hardware

The 8085 personality probe adapter is a passive hardware designed to perform the interfacing between the 8085 pinout and the KLA's data inputs. The pin assignment is listed in Table 1. Data probes 1 through 4 record all signals necessary for disassembly.

Use of data probe 4 is optional. It records the remaining signals of the 8085, if inserted into the probe rack. Otherwise, it can be used to analyse further parts of the circuit under test like the other remaining data probes, if any.

The special 8085 dedicated clock probe is used to generate the clock +J0 by oring the signals RD/, WR/ and INTA/. Data are sampled at the positiv going clock edges therefore. The input signal ALE makes up the external clock -J1 (sampling at the negativ going clock edge).

Table 1. 8085 / KLA Input Pin Assignment

Note: GND is connected to pins 2, 4, 6, 8, 10, 12, 14 and 16 of each probe, further to A-5c through A-28c and B-5a through B-28a

PROBE 1		Processor		Mother
Pin	Bit	Name	Pin	Board
1	0	DA00	12	B-1a
2	1	DA01	13	B-2a
2	2	DA02	14	B-3a
4	3	DA03	15	B-4a
5	4	DA04	16	A-4c
6	5	DA05	17	A-3c
7	6	DA06	18	A-2c
8	7	DA05	19	A-1c

PROBE 2		Processor		Mother
Pin	Bit	Name	Pin	Board
1	0	A08	21	B-1c
2	1	A09	22	B-2c
3	2	A10	23	B-3c
4	3	A11	24	B-4c
5	4	A12	25	A-4a
6	5	A13	26	A-3a
7	6	A14	27	A-2a
8	7	A15	28	a-1a

PROBE 3		Processor		Mother
Pin	Bit	Name	Pin	Board
1	0	IO/M	34	B-5c
2	1	S0	29	B-6c
3	2	S1	33	B-7c
4	3	INTR	10	B-8c
5	4	ALE	30	A-8a
6	5	SOD	4	A-7a
7	6	SID	5	A-6a
8	7	INTA	11	A-5a

PROBE 4		Processor		Mother
Pin	Bit	Name	Pin	Board
1	0	VCC	40	B-9c
2	1	HOLD	39	B-10c
3	2	HLDA	38	B-11c
4	3	CLK0	37	B-12c
5	4	TRAP	6	A-12a
6	5	R7.5	7	A-11a
7	6	R6.5	8	A-10a
8	7	R5.5	9	A-9a

PROBE J		Processor		Mother
Pin	Bit	Name	Pin	Board
1	0	RD	32	B-32c
2	1	WR	31	B-31c
3	2	INTA	11	B-30c
4	3	HLDA	38	B-29c
5	4	ALE	30	B-29a
6	5	S0	29	A-30a
7	6	S1	33	A-31a
8	7	IO/M	34	A-32a

3.2 Software

KLA / 8085 disassembler software can be devided into the functional groups described below. The trigger conditions are set in TRIGGER SEQUENCE menu and TRIGGER WORDS menu.

3.2.1 Setup

The disassembler menu is called into display by depressing <F2>. By this, the software automatically iniatializes necessary parameters for probes 1 to 3 and J. This "preset" is displayed in the different KLA menues as usual. All setting which are not compatible to the disassembler are changed. Some setup parameters control the function of the disassembler, like clock qualifying. They are set from the disassembler menu automatically, but can be set manually in the standard menues, too.

3.2.2 Filter

After taking a record, data are already in the microcomputer RAM on the KDT-6 computer board. The filter processes the control signals recorded and decides which type of bus activity, like opcode fetch, I/O- Read/Write ..., has been performed. Data are then signed appropriately.

3.2.3 Disassembler

The disassembler translates the codes recognized as opcodes into 8085 mnemonics.

3.2.4 Display Software

Data processed as described above are then displayed on the screen. You can select what type of bus activities, like opcode, memory or I/O read/write, interrupt, should be displayed. Furthermore, you can select any part of the whole stored listing.
Disassembler, display software and some special setup settings are components of the dedicated 8085 disassembler software.
Data recorded under control of this software, however, can be displayed in the well known forms of displays like timing diagram or data list, or can be used for comparisons in the COMPARE MENU as usual.

4. Operation

Taking a record is started (and can be interrupted) as usual by depressing the RUN/STOP button in any display or menu. Setting the parameters relevant for recording and analysis is described below.

4.1 Setup

Each time the disassembler is called (by depressing <F2>) the parameters necessary for the disassembler are set automatically. The parameters set that way are kept when calling other menues into display. However, they can be changed manually, of course. By this, e.g., you can enter parameters for probes 5 to 8. When pushing <RUN/STOP>, these changed parameters are valid. After calling up the disassembler, the preset values are present again.

4.2 Triggering

All settings for triggering are entered in the TRIGGER WORDS menu and the TRIGGER SEQUENCE menu as usual. All triggering features known from the KLA are kept. You only have to know the pin / channel assignment given in table 1 and the functions of the 8085, in special those of the control lines S0, S1 and IO/M.

To trigger on certain opcodes, data or addresses, we propose the following grouping in the TRIGGER WORDS menu:

Probe 1 (address/data multiplexed):	D. for Data
Probe 2 (address, high byte):	A, for Address
Probe 3 (control lines):	E

This grouping is preset in the setup 8085DIS, however it can be changed to your special needs.

By setting bits 0 to 2 in group E of the trigger word, like described in table 2 on the next page, you can select the type of bus activity to trigger on. Triggering is possible only on words which are set to be recorded in the disassembler menu (see 4.3).

Table 2.

Bus Activity	Bit 0 IO/M	Bit 1 S0	Bit 2 S1	Bits 3-7	
Opcode Fetch	0	1	1	XXXXX	
Memory Read	0	0	1	XXXXX	
Memory Write	0	1	0	XXXXX	
I/O Read	1	0	1	XXXXX	
I/O Write	1	1	0	XXXXX	
Interrupt	1	1	1	XXXXX	X = don't care

To trigger on a certain address with a certain instruction, you must trigger sequentially on 2 trigger words because of the 8085's multiplexed address / data bus. The first one contains low and high address bytes, the second one data. Both may have the setting for opcode fetch on group E (control lines). Using more than 2 trigger levels in the TRIGGER SEQUENCE menu allows you to trigger on a sequence of instructions.
Inputs not used by the disassembler (probes 5 through 8) can be used freely for further data recording.

4.3 Disassembler Menu

The disassembler menu displays the recorded data in a disassembled mode. In field mode, parameters for recording of different types of data and displaying data can be entered. Operation is the same as in the basic KLA displays LIST or TIMING. The input field offers the following choice:

(1) Record: By activating (inverse video) or deactivating (normal video) you select the type of bus activity to be recorded.

Note:
a) Triggering is only possible on data which are "on" in the record field.
b) If all record fields are switched off, nothing is recorded.
c) During DMA operation, the 8085 CPU is inactive as long as HLDA is active (high). In this state, the 8085 disassembler records no data.

(2) Display: This functions allows for selective display of recorded data. Selection as in the record field. Only data recorded previously can be displayed, of course.

(3) Memory: Like in LIST and TIMING you can select whether to display the data recorded most recently (SOURCE) or those stored in the reference memory.

(4) Roll by: INSTRUCTION or LINE selects between line by line or instruction by instruction screen move (scroll).

(5) Instr. Home: Same function as in LIST or TIMING. Enter the number of a disassembled instruction. By pushing <HOME> the disassembled listing is displayed beginning at the specified instruction. Pressing <HOME> again recalls the former part of the list into display.

4.3.1 Columns In The Disassembled Listing

(1) INSTR(ruction): The disassembled 8085 instructions are numbered. The numbering is referenced to the line with the trigger which has number 0000. Pre trigger data have negativ numbers.

(2) ADDR(ess): Contents of 8085 address bus.

(3) DATA: Contents of 8085 data bus.

(4) OPCODE: This column contains the disassembled 8085 mnemonics or a symbol for the registered bus activity:

Mem. Read	I/O Read	Interrupt	RST 5.5	RST 7.5
Mem. Write	I/O Write	Trap	RST 6.5	

4.3.2 Layout of the Data Field

(1) A maximum of 17 lines are displayed.

(2) 8085 Mnemonic and bus activity occupy one line each.

(3) The displayed page starts with the first cycle of a displayed instruction, i.e. normally with an opcode.

(4) All lines belonging to one instruction have the same number.

(5) There are 2 modes of displaying data on the screen: Instruction by instruction or line by line. In instruction mode, only instructions appear on the screen which can be displayed completetely. Therefore, there can be blank lines at the bottom of the screen if an instruction cannot be displayed completely. In line mode, however, always 17 lines are displayed.

(6) In screen mode. the disassembled data can be moved like in the LIST:

scroll up,	line by line or instruction by instruction
scroll down,	line by line or instruction by instruction
scroll left (forward)	line by line or instruction by instruction
scroll right (backw.)	line by line or instruction by instruction

(7) By depressing <HOME>, you switch from the listing displayed presently to the instruction given in the <HOME> field.

(8) The first displayed line of the disassembled listing corresponds to the start magnifier of LIST and TIMING.

5. Data List And Timing Diagram

The contents of the data memory can be displayed as usual as data list or timing diagram. All functios explained in the KLA operating manual can be used. Start magnifier S, trigger T and cursor C in all 3 diagrams are on the same addresses.

6. Installing The 8085 Disassembler

(1) Switch off the KLA.

(2) Place 8085 configurator module on UPR probe rack. Consider connector codes!

(3) Plug ribbon cable with CPU adapter (40 pin clip) to configurator. Consider connector codes!

(4) Carefully plug probes 1, 2, 3 and J-8085 into the marked locations inside the UPR.

ATTENTION!

The probes fit into the connectors inside the UPR very softly if inserted correctly. Do not use power, as some of the probe's pins might bend and a repair might be necessary subsequently. The probe is inserted correctly if the long sticker tape on top of the probe case is on the same side as the labelling for the probe inside the UPR. This applies for all probes.

(5) Connect probes to their appropriate places on the KLA's rear side.

(6) Place 40 pin clip on CPU. Look for correct pinning. Pins 1 of both CPU and clip are marked.

(7) Switch the KLA on.

(8) Load KLA / 8085 disassembler software.

(9) Call disassembler menu into display with key <F2>.

APPENDIX

Multiclock Probe (PCB475Rev1.1M2)

The multiclock probe is a more advanced KLA logic probe dedicated to applications where the normal KLA data / clock probe cannot be used conveniently. It is required for use with the KLA disassemblers for 8085 and 68000 CPUs.

The multiclock probe combines up to 8 inputs. By setting jumpers, it is possible to implement 4 boolean functions: OR, NOR, NAND, AND.

If 2 clocks are required, each 4 inputs can be grouped to one clock.

Configuring the multiclock probe:

Jumpers J1, J2, J4, J5, J7, J8, J11 and J12 (please refer to schematic diagram and parts locations drawing for input channel / jumper assignment) are used to select inverted or non-inverted operation of the appropriate channel. Jumper position 1-2 = non-inverted, 3-2 = inverted. Channels 0 to 3 and channels 4 to 7 are fed to 4 input ORs/NORs to allow ORing of clocks. Jumpers J6 and J9 select OR / NOR operation of these gates. Closing J3 allows ORing of all 8 inputs in a wired-OR configuration.

To change jumper positions, open the 4 screws of the probe's case. Refer to the table listed below and to the schematic diagram and parts locations drawing to set jumpers according to your needs.

Jumper positions: (Jumpers not listed are not relevant)

	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13
8 channel wired OR:													
no 8 channel ORing			3-2							1-2			1-2
(I4+I5+I6+I7) non-inv.			1-2						1-2	3-2			1-2
(I4+I5+I6+I7) inverted			1-2						1-2	1-2			3-2
8085	3-2	3-2		3-2		1-2		1-2	3-2	1-2			1-2
68000	3-2	3-2				3-2			3-2	1-2			1-2

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KONTRON MESSTECHNIK GMBH · Breslauer Strasse 2
D-8057 Eching/Munich · Phone (089) 31901-0 · Telex 522122